

AN-1077 Application Note

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Figure 2. Output Response vs. Orientation to Gravity

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ELECTRICAL CONNECTION

ADXL345 communication is done via either I²C or SPI (3or 4-wire mode). Figure 3 shows the recommended electrical connections for 4-wire SPI mode. Note that the SDO pin can be disconnected when using 3-wire SPI mode.

Figure 4 shows the recommended electrical connection for I²C mode. The 7-bit I²C address for the device is 0x53, followed by the R/W bit. The user can select an alternate I²C address by connecting the SDO/ALT ADDRESS pin to the V_{DD I/O} pin. The 7-bit I²C address for that configuration is 0x1D, followed by the R/W bit.

Refer to the ADXL345 data sheet for details on power supply decoupling.



Figure 3. Recommended Connection for 4-Wire SPI Mode



Figure 4. Recommended Connection for I²C Mode

COMMUNICATION INTERFACE

Table 1 gives the list of typical configuration settings for the master processor requirements for SPI communication with the ADXL345. These settings are normally in control registers. Refer to the ADXL345 data sheet for timing specification and a command sequence.

Table 1. SPI Settings

Processor Setting	Description			
Master	ADXL345 operates as slave			
SPI Mode	Clock polarity (CPOL) = 1			
	Clock phase (CPHA) = 1			
Bit Sequence	MSB first mode			

For I²C communication, refer to the ADXL345 data sheet and *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007 for processor settings as well as timing specifications and a command sequence.

Sometimes it is important to confirm the validity of a communication sequence before going to the next design stage. This can be done by reading the DEVID register (Address 0x00). It is a read only register that contains 0xE5. If the data read from DEVID is not 0xE5, it is the indication that either the physical connection or command sequence is incorrect.

INITIALIZATION

Figure 5 shows the minimum initialization sequence. The ADXL345 operates in a 100 Hz ODR with a DATA_READY interrupt on the INT1 pin during this start-up sequence. When setting other interrupts or using the FIFO, it is recommended that those registers used are set before the POWER_CTL and INT_ENABLE registers. Refer to the ADXL345 data sheet and the AN-1025 application note for other operation modes of ADXL345 and details about FIFO.



Figure 5. Minimum Initialization Sequence

READING OUTPUT DATA

The DATA_READY interrupt signal indicates that 3-axis of acceleration data is updated in the data registers. It is latched high when new data is ready. (The interrupt can be configured to be latched from low-to-high through the DATA_FORMAT register. Refer to the ADXL345 data sheet for details.) Use the low-to-high transition to trigger action on an interrupt service routine. Data is read from the DATAX0, DATAX1, DATAY0, DATAY1, DATAZ0, and DATAZ1 registers. To ensure data coherency, it is recommended that multibyte reads are used to retrieve data from the ADXL345. Figure 7 shows the read sequence example for 4-wire SPI.

DATA FORMAT

The data format of the ADXL345 is 16 bits. Once acceleration data is acquired from data registers, the user must reconstruct the data. DATAX0 is the low byte register for X-axis acceleration and DATAX1 is the high byte register. In 13-bit mode, the upper 4 bits are sign bits (see Figure 6). Note that

other data formats are available by setting the DATA_FORMAT register. See the ADXL345 data sheet for more details.

The ADXL345 uses twos complement data format. When in 13-bit mode, 1 LSB represents about 3.9 mg.

1						
16-Bit Code (Hex)	Twos Complement Representation (Dec)	Acceleration (mg)				
OFFF	4095	+1599				
0002	+2	+7.8				
0001	+1	+3.9				
0000	0	0				
FFFF	-1	-3.9				
FFFE	-2	-7.8				
F000	-4095	-1600				



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USING THE SELF-TEST FEATURE

The ADXL345 provides a self-test feature that enables an electromechanical test on the device without external mechanical stimulus. Figure 8 outlines a recommended self-test sequence. Note that the ADXL345 should be placed in a stable environment when conducting the self-test sequence.



Figure 8. Self-Test Sequence

USING OFFSET REGISTERS

The ADXL345 has offset registers that facilitate offset calibration. The data format for the offset registers is 8-bit, twos compliment. The resolution of the offset registers is about 15.6 mg/LSB. If offset calibration must be finer than 15.6 mg/LSB, the calibration needs to be done at the processor. The offset register adds the value written in the register to measured acceleration. For example, if the offset is +156 mg, then

START

-156 mg should be written to offset register. Figure 9 shows the typical offset calibration sequence.

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For this routine, X/Y axes errors are zero when 0 g input is applied, whereas Z-axis errors are zero when 1 g input is applied. Greater accuracy can be achieved if it is possible to rotate the ADXL345 at calibration.

	_					
PLACE SENSOR IN X = 0g, Y = 0g, Z = +1g ORIENTATION						
•						
$V_{S} = ON$ $V_{DD I/O} = ON$						
•			DECISTED	DECISTED		
WAIT 1.1ms]	STEP	ADDRESS	NAME	DAT	A DESCRIPTION
•		1	0x31	DATA_FOR	MAT 0x0E	±16g, 13-BIT MODE
	1	2	0x2D	POWER_CT	L 0x08	START MEASUREMENT
SEQUENCE	>	3	0x2E	INT_ENABL	E 0x80	ENABLE DATA_READY INTERRUPT
*						
WAIT 11.1ms]►	WHEN AT ODR = 100Hz (WAIT TIME DEPENDS ON ODR SETTLING AND 1.1ms + 1/QDR)				
•						
TAKE 100 DATA POINTS AND AVERAGE		> IT IS TO MINIMIZE THE EFFECT OF NOISE				
└─── ∀	1	$X_CALIB = -(OUTPUT (X) \div 4)$				
CALCULATE CALIBRATION VALUE	►	Y_CALIB = -(OUTPUT (Y) ÷ 4) Z_CALIB = -((OUTPUT (Z) – 256) ÷ 4)				
•	-					
WRITE TO OFSTx REGISTERS	}►	STEP	REGISTER ADDRESS	REGISTER NAME	DATA	DESCRIPTION
*	_	1	0x1E	OFSTX	X_CALIB	X_CALIB TO BE 8 BIT
	`	2	0x1F	OFSTY	Y_CALIB	Y_CALIB TO BE 8 BIT
)	3	0x20	OFSTZ	Z_CALIB	Z_CALIB TO BE 8 BIT

Figure 9. Offset Calibration Sequence

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